A 2 to 8 GHz LEVELING LOOP USING A GaAs MMIC ACTIVE SPLITTER AND ATTENUATOR

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ABSTRACT

A wide-band monolithic GaAs bridged-T variable attenuator has been used with a monolithic GaAs active power splitter to form a compact, 2 to 8 GHz leveling loop for RF sources having a minimum 12dB leveling range with buffered output. The attenuator internally optimizes input and output return loss over a 1 to 10 GHz bandwidth by the use of an on-chip GaAs op-amp. The active power splitter provides unity gain to each port over a 1 to 10 GHz bandwidth by the use of distributed amplification. The entire 4.5 cm by 4 2 cm subsystem was realized with surface mount packages on RT-Duroid®.

INTRODUCTION

GaAs MMIC's have recently moved out from the development stage and into the marketplace. The majority of MMIC's currently available are gain blocks, with only a few exceptions. The additional microwave "building blocks" are not yet available, mainly because of the application specific nature of microwave design. Because GaAs MMIC's need to address a broad spectrum of applications and bandwidths, their design and function must be carefully chosen. Otherwise, the volume of MMIC's will not realize the lower price per component which is the goal of moving circuits to the monolithic level. Two such generic microwave components are presented here in a practical, broadband microwave leveling loop.

The design approach used allowed a broad bandwidth operation of 1 to 10 GHz for both the attenuator and splitter MMIC's. The MMIC's were fabricated with a high yield, 1 micron, GaAs depletion mode ion-implantation process [1], incorporating NiCr resistors for stable terminations and MIM capacitors for on-chip bypassing and decoupling. Inductors used second layer air-bridge metal to reduce skin effect losses and increase the self resonant frequency. Both parts were designed for operation from a single 9 to 15 V power supply for ease of use and incorporation into existing system environments. A die size of 54 by 43 mils was chosen for both circuits to fit into a hermetic, surface mount package already developed and demonstrated [2].

The design and performance of each of the MMIC's is described separately, and together in the leveling loop application, demonstrating the packaging and use of broadband MMIC's in microwave subsystems.

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VARIABLE ATTENUATOR

Gain control of amplifier cascades generally require a variable attenuator element. For amplifier stability, it is desirable that the attenuator provides constant source and load match regardless of the attenuation value This rules out reflective attenuator topologies. The classic bridged-T attenuator, shown in Fig. 1, becomes a continuously variable absorptive attenuator when R_1, the series bridging resistance, and R_2, the shunt resistance are allowed to vary as follows:

$$R_1 R_2 = Z_0^{\,2} \tag{1}$$

where Z_0 is the desired characteristic impedance. The attenuation when matched is given by:

$$\textit{attenuation (dB)} = 20 \log \left((R_1/R_2)^{1/2} + 1 \right) \tag{2}$$

By replacing the series and shunt resistances, R_1 and R_2, with FET's operating in the linear region, a monolithic implementation of the bridged-T attenuator, shown in Fig. 2, has been realized. The channel resistance of a FET in the linear region is essentially $1/g_m$ from the saturated region, which can be varied by V_{gs}:

$$I_{ds} \approx 2\frac{W}{L}\beta_0 \left(V_{gs} - V_p \right) V_{ds} \approx g_{m_{SAT}} V_{ds} \tag{3}$$

The transconductance parameter, β_0, is given as $\beta_0 = (\mu \epsilon_s / 2a)$ where μ is the channel electron mobility, ϵ_s is the permittivity of the GaAs, and a is the channel thickness. It can be seen from (3) that the channel resistance, $(\partial I_{ds}/\partial V_{ds})^{-1}$, is dependent on GaAs process spreads, influencing both β_0 and V_p. The task then is to control the product of series and shunt channel resistances for proper attenuator operation. Solving for the necessary applied FET gate voltages, V_{gs_1} and V_{gs_2}, suggests the following transfer

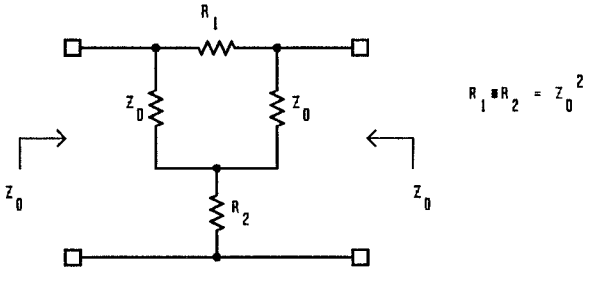

Fig. 1. The bridged-T attenuator.

function for maintaining good return loss at any given attenuation for FET's of equal geometry:

$$\left(V_{gs_2}-V_p\right)=\frac{Z_0^2L^2}{4W^2\beta_0^2\left(V_{gs_1}-V_p\right)} \tag{4}$$

Fortunately, feedback can be used to control input and output return loss as attenuation is changed, invariant of any process effects or differences between FET geometries. Fig. 2 shows the reference attenuator cell where an operational amplifier adjusts the shunt FET gate voltage in response to an arbitrary voltage variation on the series FET gate, maintaining a 50 ohm environment. Before the MMIC attenuator was designed, the concept of using feedback to measure DC parameters of an attenuator cell and match the RF parameters was verified by using two GaAs FET bridged-T attenuators and a 741 operational amplifier. This concept was carried to the monolithic level by implementing the op-amp on chip.

Several factors have to be considered when using FET's for the shunt and series elements. FET widths must be chosen wide enough for low insertion loss at the minimum end of the attenuation range, but small enough to limit parallel drain-to-source capacitance, C_{ds}, so that the isolation at higher frequencies is sufficient. Both series and shunt widths were chosen as 300 microns. The isolation is most dependent on C_{ds} of the series FET, so this device was built

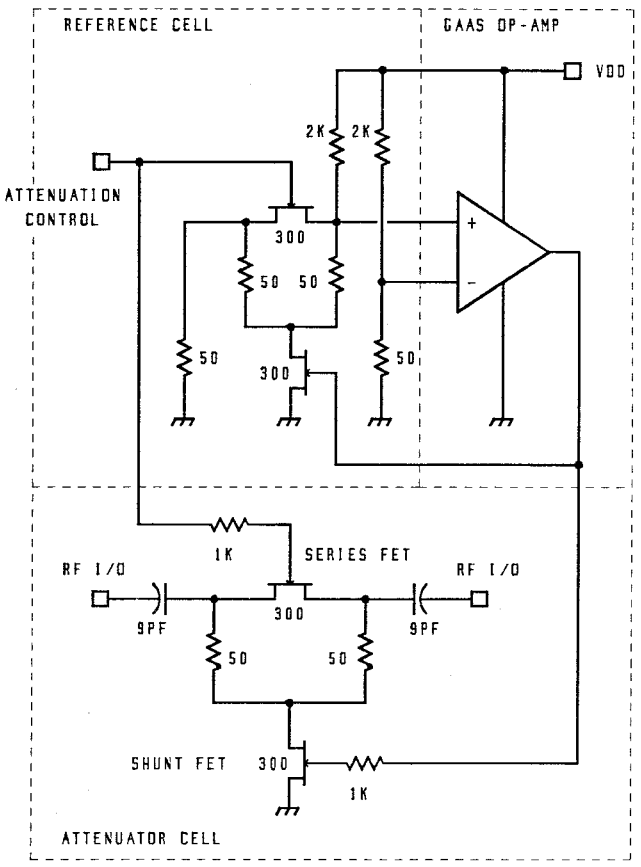

Fig. 2. Monolithic 1 to 10 GHz variable attenuator using GaAs FET's in the bridged-T configuration.

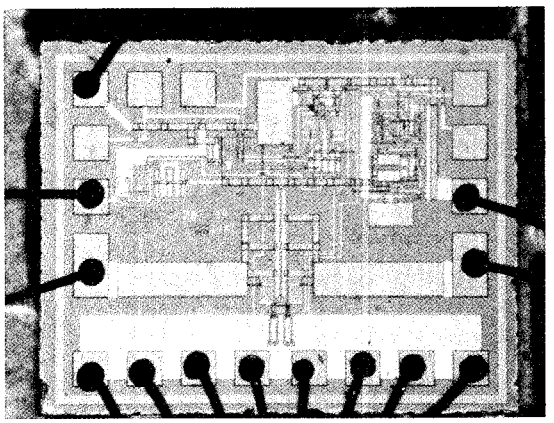

Fig. 3. Microphotograph of the 1 to 10 GHz variable attenuator. The op-amp is visible in the upper right corner.

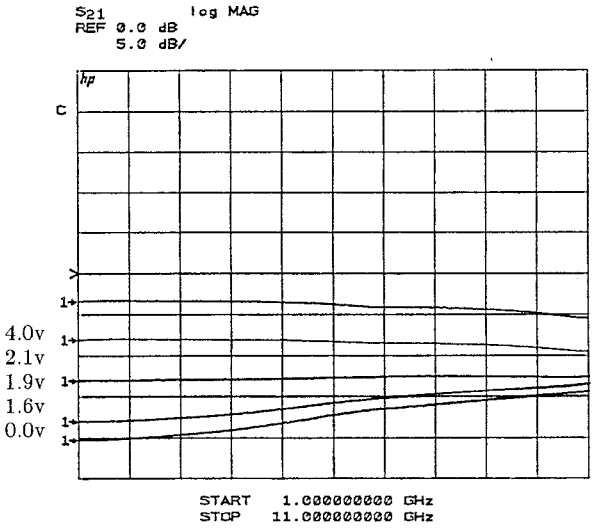

Fig. 4. Attenuation vs. frequency for varying control voltages.

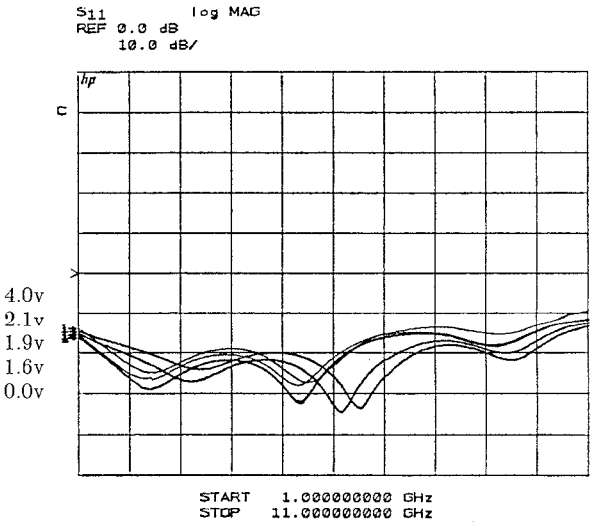

Fig. 5. Input return loss vs. frequency for various attenuations using on-chip match optimization scheme.

as a single gate finger device to reduce additional drain-to-source capacitance caused by the interconnection parasitics which occur in interdigitated structures. The losses associated with the single gate finger series device do not effect the RF performance of the attenuator. A photograph of the attenuator MMIC is shown in Fig. 3.

Fig. 4 shows the transmission characteristics of the packaged attenuator. The gain slope at minimum attenuation is caused by combined losses due to the package and microstrip structures on the GaAs to control the impedance from the edges of the die to the attenuator cell. Minimum insertion loss is 3.5dB at 1GHz increasing to 5dB at 10GHz. In this design, the gate-to-source voltage of both FET's was never allowed to exceed V_{gs}=0. If V_{gs} is allowed to go positive near the forward conduction point, insertion loss will improve by approximately one dB. The effect of C_{ds} upon the isolation increases visibly at higher frequencies. Attenuation range is 32dB at 1GHz decreasing to 10dB at 10GHz.

Fig. 5 shows the return loss as a function of frequency using the on-chip correction circuitry. Return loss exceeds 12 dB over the 1 to 10GHz band, translating to a better than 1.7:1 VSWR for the packaged part. This performance démonstrates that the addition of complex analog biasing circuits can be used to bring increased functionality to GaAs MMIC designs.

ACTIVE POWER SPLITTER

A novel active power splitter provides unity gain to each port over the 1 to 10 GHz band through the use of distributed amplification. Two distributed amplifiers share a common input line to provide dual outputs without the need for lossy or band-limiting passive dividers (Fig. 6). The inherent symmetry of the topology provides close amplitude and phase match between outputs. This concept, in theory, can be extended to N outputs, or with dual-gate FET's, to switchable outputs. Unequal power division is possible with unequal side to side FET periphery.

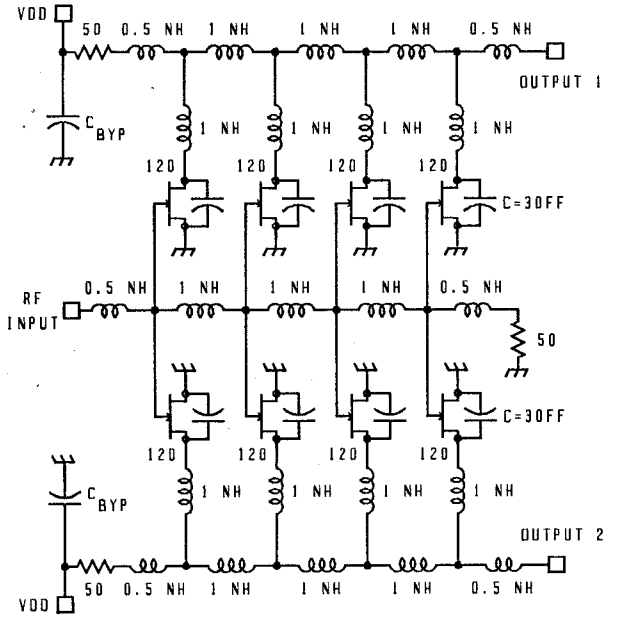

Fig. 6. Active splitter using distributed topology and common input gate line.

The combined input capacitance of two 120 micron FET's forms the shunt reactance element of the lumped equivalent 50 ohm input line. The four sections yield a total gate periphery of 480 microns per side. The devices operate at I_{DSS} for maximum power gain and require 100 mA total current from a single 8 to 15 volt power supply. Because the FETs are spread out over the die area with only two fingers interdigitated at their closest spacings, operation at I_{DSS} was not viewed as a serious reliability problem, especially because the package was designed to handle 1 to 1.5 watt dissipation levels. This provides a maximum possible gain per side of $g_m R_l/2$ of 1.3dB before including finite inductor Q and packaging losses. These losses were partially compensated at the high end by adding series drain inductance to peak the overall response and introduce some slight positive gain slope in the unpackaged part. This peaking occurs from the inductors tending to impedance match the FET outputs at high frequencies. Fig. 7 shows a photo of the splitter MMIC.

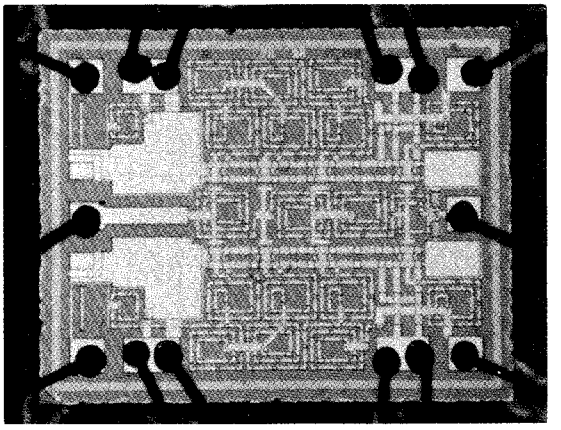

Fig. 7. Microphotograph of the 1 to 10 GHz active power splitter.

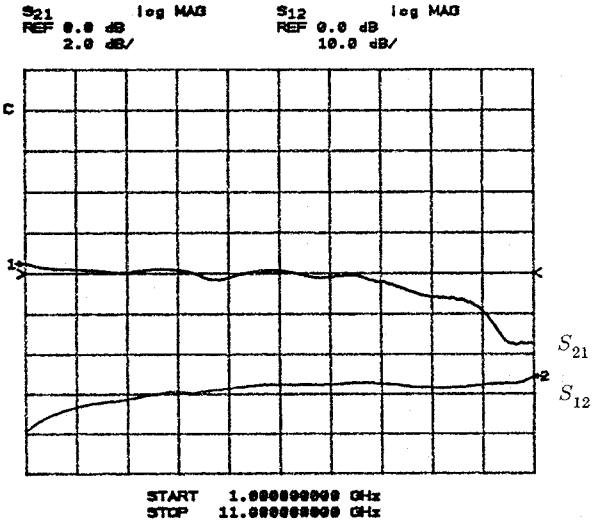

Fig. 8. Active splitter transmission characteristics. Note that S_{21} is shown at 2dB/div.

Fig. 8 shows the transmission characteristics of the splitter. Packaged gain flatness was ±1dB over 1 to 10 GHz, with less than ±0.5dB over the 2 to 8 GHz band. Reverse isolation was greater than 27dB from 1 to 10 GHz Packaged input and output VSWR's, shown in Fig. 9, were better than 2 1, typical of the broadband performance of distributed amplifiers. Packaged output amplitude and phase balance over 1 to 10 GHz were less than ±0.4dB and ±1.5 degrees, respectively. Output port-to-port isolation exceeded 24dB up to 9 GHz, decreasing to 20dB at 10GHz as shown in Fig. 10 One dB compressed power output was measured at greater than +10dBm. This level of performance was achieved by using the symmetry incorporated into the surface mount package design [2].

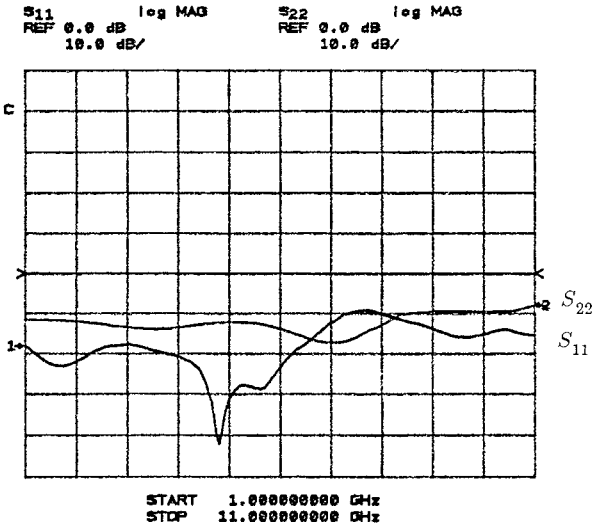

Fig. 9. Active splitter reflection characteristics

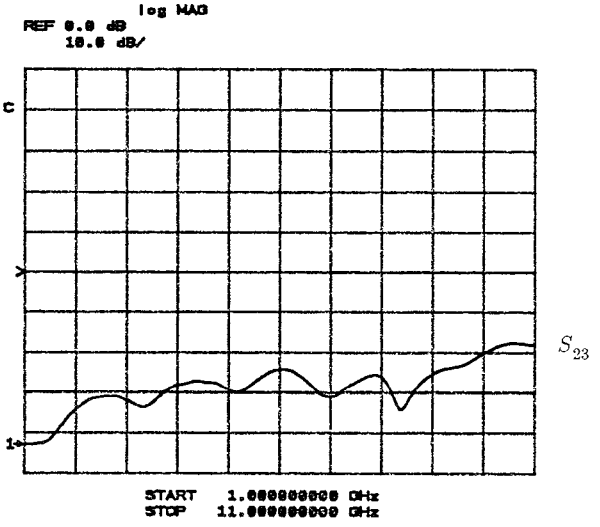

Fig. 10. Output port-to-port isolation for the packaged active splitter.

LEVELING LOOP SUBSYSTEM

The two GaAs MMIC's were used as the key components to build a 2 to 8 GHz leveling loop subsystem. Fig 11 shows the block diagram of the leveling loop. The external operational amplifier is used for the loop gain element in addition to the attenuator internal op-amp which controls its input match. The only off-board component used in the subsystem is a wide band coaxial detector All other components were surface mounted as shown in Fig. 12.

Improvement of the overall isolation results from the contribution of the splitter. The use of the active splitter allowed one output port to be used for the detector controlling the attenuator while the second port simultaneously provided the buffered output of the leveled source Since output port-to-port isolation is high, mismatches in the leveled output port do not influence the feedback path to the attenuator and a stable loop results The ultimate leveling range of the loop is set by the attenuation range of the attenuator MMIC at the highest frequency of operation desired. At 8GHz, this range was measured at 12dB RF source isolation was in excess of 30dB using the design topology presented here. Fig. 13 shows a typical response of the leveling loop in operation from 2 to 8 GHz. The source was an unleveled, swept YIG oscillator whose amplitude characteristics are visible in the top trace in the photo. The leveling loop utilized dominant pole compensation to set the loop bandwidth to approximately 100KHz. This was sufficient to accommodate the relatively slowly varying power ripples in the YIG oscillator at it's maximum sweep rate of 2 5 msec/Ghz.

The packaged GaAs MMIC's were surface mounted on a 4.5cm by 4 2cm RT-Duroid® board, 31 mils thick, to form the leveler subsystem shown in Fig. 12 For demonstration of the leveling loop, SMA connectors provided input and output ports, with coplanar transmission lines between the MMIC's. In typical application, these input and output connections would come from other surface mount components. A backside aluminum plate provides rigidity for the soft substrate, as well as thermal heat sinking for the active components.

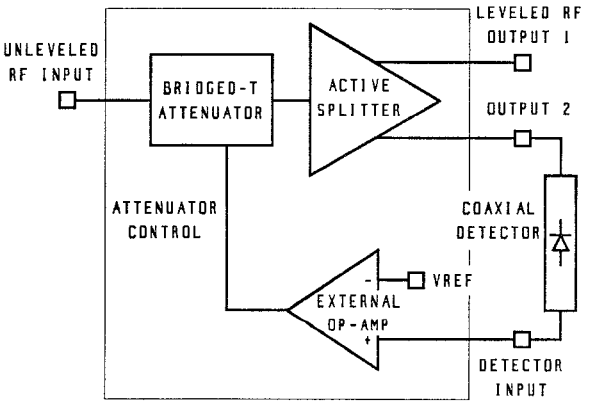

Fig. 11. Block diagram of the leveling loop subsystem.

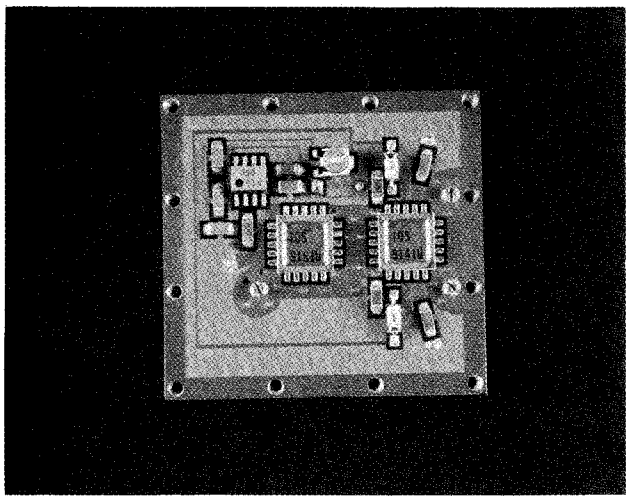

Fig. 12. Photo of the leveling loop subsystem showing the surface mounted GaAs MMIC's.

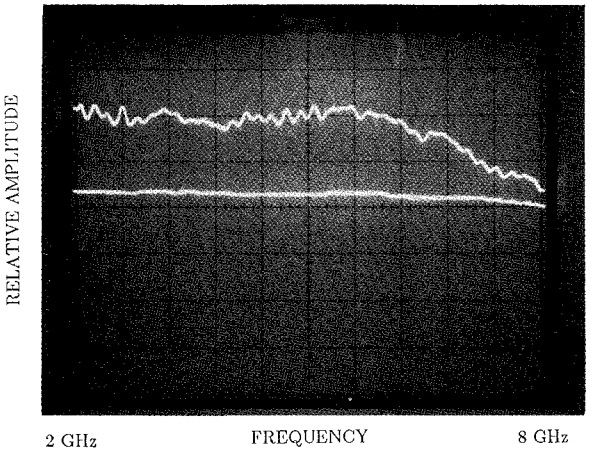

Fig. 13. Operation of the leveling loop over the 2 to 8 GHz band. The input source is shown before (upper trace) and after leveling (lower trace). The vertical scale is 5dB/div.

CONCLUSIONS

A 2 to 8 GHz leveling loop has been demonstrated which shows the application of new generation designs using GaAs MMIC's. More than 30 dB of source isolation and 12 dB leveling range at 8 GHz are attributed to the design and application of a GaAs variable attenuator and an active power splitter.

The novel attenuator circuit shown here is the first reported application of an on-chip GaAs operational amplifier to internally optimize the input and output return loss as the attenuation is varied. Packaged input and output VSWR is held to better than 1.7:1 over the entire 1 to 10 GHz band. Furthermore, this performance demonstrates that the addition of complex analog circuits can be used to bring increased functionality to GaAs MMIC designs.

The active splitter uses two distributed amplifiers sharing a common gate line to provide flat unity gain over the 1 to 10 GHz range with reverse and port-to-port isolations exceeding 27dB and 20dB, respectively. Input and output VSWR's were better than 2:1, typical of the distributed amplifier topology.

Finally, the use of surface mount packaging technology for GaAs MMIC's and soft substrate boards are projected to reduce the design time and ultimate cost of microwave systems.

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